

Supplemental Form PTO-1449 (Modified)		Attorney Docket No.:	Serial No.:
		FIS920030185US1	10/605,167
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)		Applicant: D. Chidambaram, et al.	
		Filing Date: September 12, 2003	Group: 2822
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**OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)**

<i>REP</i>	Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
<i>REP</i>	Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
<i>REP</i>	Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
<i>REP</i>	F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
<i>REP</i>	Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
<i>REP</i>	A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
<i>REP</i>	K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

EXAMINER	DATE CONSIDERED
	5-20-04

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.